Smart RFIC: Millimeter-Wave Gigabit Transceiver with Digitally-enabled Build-in Self-healing and Auto-switching Functions

Jenny Yi-Chun Liu, Ian Huang, Yen-Hung Kuo, Wei-Tsung Li, Wei-Heng Lin, Wen-Jie Lin, Jeng-Han Tsai, Hamed Alsuraisry, Saleh Alsaif, Tian-Wei Huang, *Fellow, IEEE*

I. Introduction

Everyone wants and enjoys a smart life with a smart phone, smart car, and smart home. The major difference between a smart phone and a traditional mobile phone is the user-defined functions inside the smart phone. The user can change their smart phone into a music player, a movie theater, or their own personal workstation. All functions can be defined by the user with all flexibility.

For a smart car, if there are more sensors such as video sensors, LiDAR sensors, or even millimeter-wave radar, then this automobile can then be an autopilot smart car. Therefore, if there are more user-defined functions or more sensor capabilities inside the Radio Frequency Integrated Circuits (RFIC), then we can call this RFIC a smart RFIC, which is essential when facing the changing environment.

Traditionally, auto-gain control (AGC) can be easily implemented inside a RFIC for the amplitude sensing capabilities. If we have frequency and phase sensing capabilities, then our circuit will be capable of automatic band-switching and phase adjustment.

We typically have an AM radio and FM radio that uses amplitude modulation and frequency/phase modulation, respectively. To implement a quadrature amplitude modulation (QAM) digital radio, we need both amplitude and frequency/phase modulation techniques to achieve adaptable constellation with process, voltage, and temperature (PVT) variations.

II. Frequency Sensing: Auto-Band-Switching Ultra-Broadband RFIC

The function of a frequency sensor is to detect whether an input frequency is in-band or out-of-band, as shown in Fig. 1. We usually need a tunable frequency source to approximate and close in on the unknown input frequency, which requires extra dc power consumption and tuning time. Our proposed design uses a coarse band-switching sensor for fast in-band or out-of-band discernment. During our research on a Miller divider, we discovered that the divider can be used as a band-switching sensor.

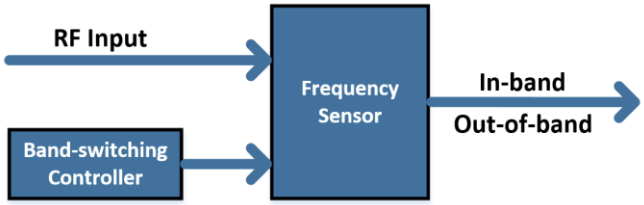
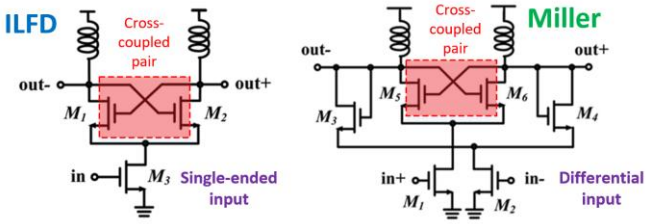


Fig. 1. A band-switching controller can switch to the correct frequency by determining if the input is in-band or out-of-band when using the Miller frequency divider.

Using Miller Dividers as a Frequency Sensor

As shown in Fig. 2, Injection Locked Frequency Divider (ILFD) is a single-ended input to a cross-coupled CMOS resonator while a Miller frequency divider is a differential input to a cross-coupled CMOS resonator. ILFD has a self-oscillating feature that generates a self-oscillating free-running output when there is no input. A Miller divider has a non-self-oscillating feature that generates no output when there is no input.



(a) (b)

Fig. 2. a) ILFD divider; b) Miller frequency divider [1].

When there is an in-band input, both frequency dividers can generate locked half-frequency large output signals under the frequency locking condition. However, for both the ILFD or the Miller divider, when there is an out-of-band input, the ILFD will generate a large multi-tone waveform because of the unlocked circuit behavior while the Miller divider will generate a small harmonic output.

Therefore, when using the Miller frequency divider, we can design a sensor to distinguish if the signal is either in-band or out-of-band. When the input signal is in-band, there will be a large amplitude output; when the signal is out-of-band, there will only be a small harmonic output. A frequency sensor can then be designed with an amplitude detector cascaded with a Miller divider as seen in the photograph of the chip shown in Fig. 3.

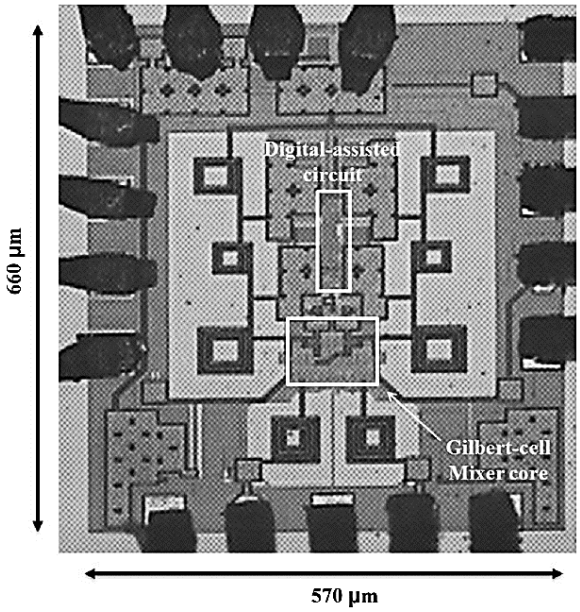


Fig. 3. Photograph of the proposed Miller frequency divider [1].

The frequency-band switches inside the Miller divider are controlled by a finite-state machine with the following sequential steps shown in Fig. 4. We can not only detect the input signal within the blue (1), red (2), or green (3) band, but we can also switch the corresponding operation of the circuit blocks such as the Low Noise Amplifier (LNA), Mixer, or Power Amplifier (PA), to the correct band to optimize the circuit performance. This three-band frequency sensor can complete the detection and switching actions within 40 ns and under 12 mW. For example, the control signals can be used to change the state of the tunable neutralization transmission lines to adjust the operation frequency of an amplifier [2]. We can then have broadband circuits built upon each band-limited block. The frequency sensing and controlling techniques can also be applied to the front-end circuits in multi-band applications or software-defined radios with fast frequency hopping capability.

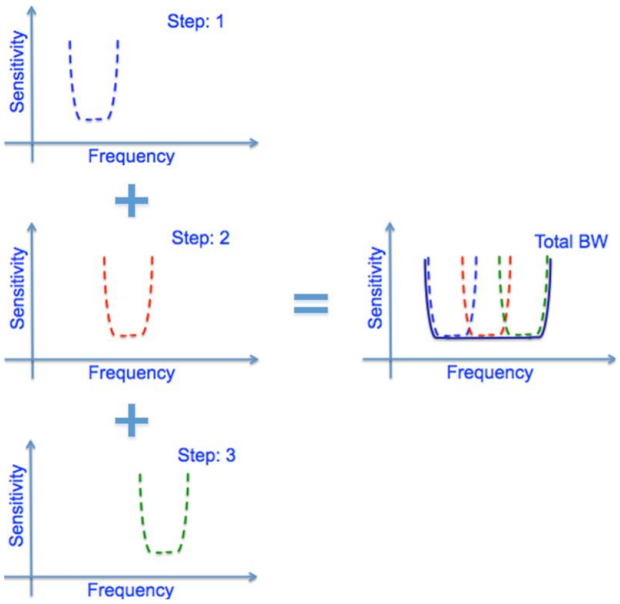


Fig. 4. A frequency sensor that covers the entire bandwidth has a coarse band-switching function to determine if the input is within any of these three bands.

III. Amplitude Sensing: Single Antenna Radar with On-Chip Isolator

For a single-antenna radar transceiver, the Transmitter-to-Receiver (Tx-to-Rx) leakage signal will degrade the receiver sensitivity. The proposed solution to cancel the leakage signal is to use a passive approach using a feedforward technique with a digitally-calibrated method, as shown in Fig. 5.

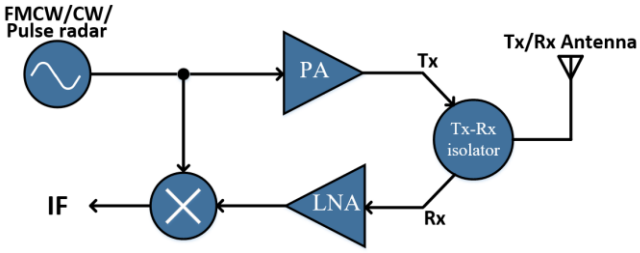


Fig. 5. Single antenna radar with on-chip isolator [3].

A feedforward technique shown in Fig. 6 is needed to improve the isolation from 15 dB to 21 dB by using an out-of-phase auxiliary signal with the same amplitude as the leakage signal to cancel the leakage signal. A digital-calibrated method is implemented to eliminate the need for a manual fine-tuning mechanism for attenuators and phase shifters and to mitigate the productions issues caused by process, voltage, and temperature (PVT) variations when designing with the analog feedforward technique.

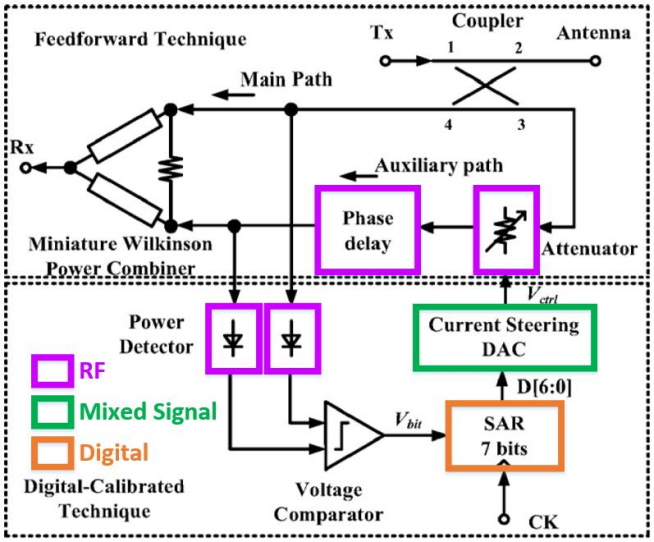


Fig. 6 Block diagram of a digital-calibrated feedforward Tx-to-Rx isolator [3].

The feedforward circuit mainly focuses on the leakage signal from the transmitter to the receiver. To cancel the leakage signal in the circuit, an auxiliary signal is introduced. The amplitude of the auxiliary signal is adjusted by using a T-type resistor network. Isolation between the main and auxiliary paths is achieved by using a Wilkinson power combiner. A way to improve the isolation at the Rx port when combining the main and auxiliary signal is an issue that requires tuning of the attenuator, so we will also incorporate a digitally-calibrated design for attenuator control.

To fine-tune the attenuator, a signal is injected at the target frequency so both the main and auxiliary path have

the same signal. Power detectors then sense and convert the amplitude of two-path signals to dc voltage. After comparing the voltages, the successive-approximation-register (SAR) circuit then records the binary signal. SAR then performs a binary search of optimal attenuation to find the optimal code word to control the attenuator through a digital-to-analog converter (DAC), as shown in Fig. 7.

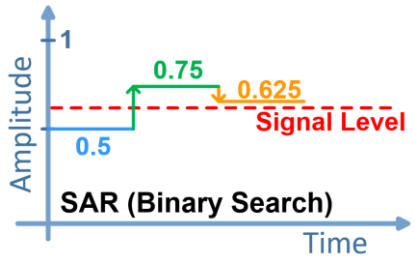


Fig. 7. Digital AGC using SAR and DAC.

The proposed IC design is implemented in a standard mixed signal and the RF 0.18 μm CMOS technology. The Tx-to-Rx leakage signal can be cancelled by the auxiliary signal using feedforward circuits with a digital-calibrated technique, which improves the isolation from around 18 dB to 27.3 dB at 25 GHz while using 13.5 mW dc power. A similar concept of amplitude sensing is adopted in LNAs and PAs. In LNAs, the received signal strength indicator, error amplifier, and loop filter form the feedback circuit for gain control that allows the LNA to operate in different gain modes [4]. In PAs, the power detector is used to sense the operation power, so it can adaptively optimize its efficiency [5]-[6].

IV. Phase Calibration: Digital Phase Shifter

Phase shifters are a critical block in phased-array systems and can be also used as tuning knobs for smart RFICs. Insertion loss, phase and gain errors, phase coverage, power consumption, and chip area are the main considerations in a phase shifter design. Passive phase shifters are commonly seen and utilized for their low dc power consumption and high linearity [7]-[9]. This passive type of phase shifter usually consists of filters and resonators with digital control. To compensate high insertion loss and gain and phase variations, a phase-invariant and gain-compensation variable gain amplifier (VGA) is necessary and can be designed using multiple amplifier stages with opposite phase variation in different phase shifting modes [10]-[11].

To reduce the phase error, phase and gain variation, and the phase-tuning complexity in a phased-array system, a 57-to-64-GHz low phase-error 5-bit switch-type phase shifter is designed with a low phase-variation VGA using 90-nm CMOS low-power technology, shown in Fig. 8 and Fig. 9. The developed 5-bit phase shifter only has a 2° RMS phase error while the VGA only has a 1.86° phase variation.

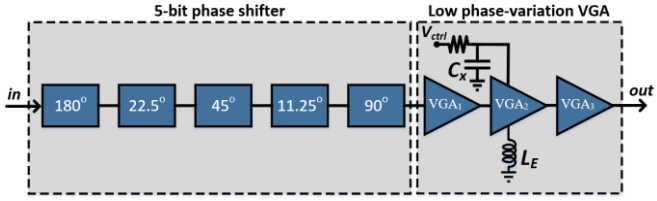


Fig. 8. Block diagram of the proposed 60-GHz 5-bit phase shifter and low phase-variation VGA [12].

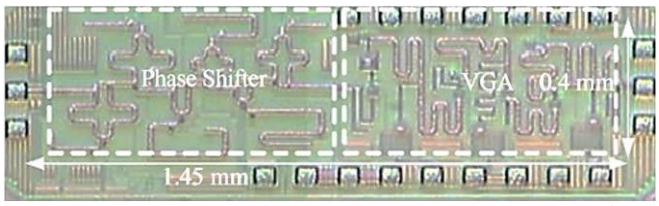
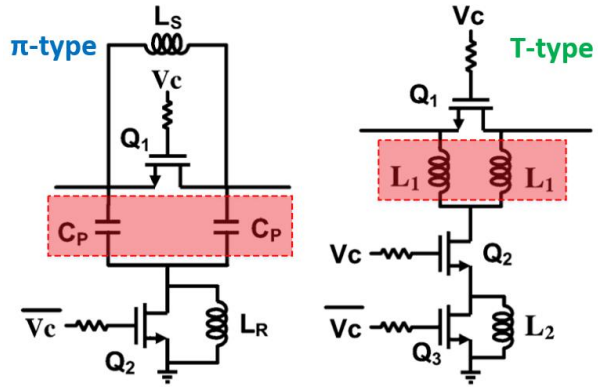


Fig. 9. Chip photograph of the 5-bit 60-GHz switch-type phase shifter and VGA [12].

5-bit Low Phase-variation Phase Shifter and Low Phase-variation VGA

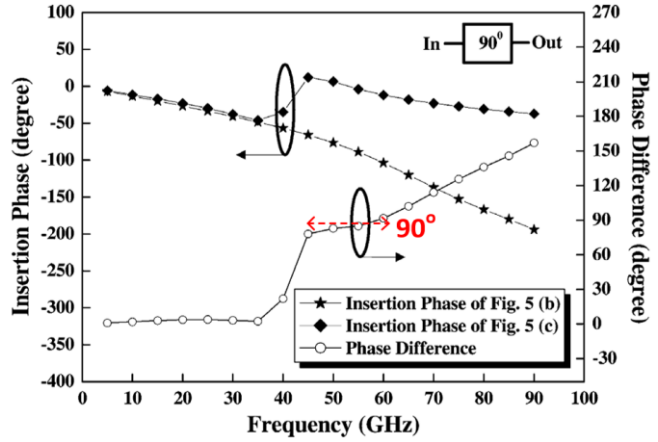
A previous study [13] shows that a 4-bit switch-type phase shifter can achieve a low phase-variation of 2°. For our current 5-bit phase shifter, we have sequenced the phase-shifting stages by cascading 180°, 22.5°, 45°, 11.25°, and 90°, respectively, to reduce the loading effects from adjacent stages.

When comparing a T-type to a π-type switch-type phase-shifting stage, the T-type stage shown in Fig. 10 was chosen and used due to the improvements regarding phase linearity and group delay. A comparison of the two showed that the T-type has a much wider bandwidth than the π-type phase shifter for 90° phase shifting, as shown in Fig. 11(a) and (b). When comparing the group delays for these two switch-type phase shifters, we can see that the π -type and the T-type phase shifters has a group delay deviation of 6.5 ps and 0.8 ps, respectively, between V_c = 0V and V_c = 1.2V, as shown in Fig. 12(a) and (b). Having less group delay for a broadband signal means that there is less phase error, so a T-type phase shifter was implemented because of its better phase linearity and smaller group delay.

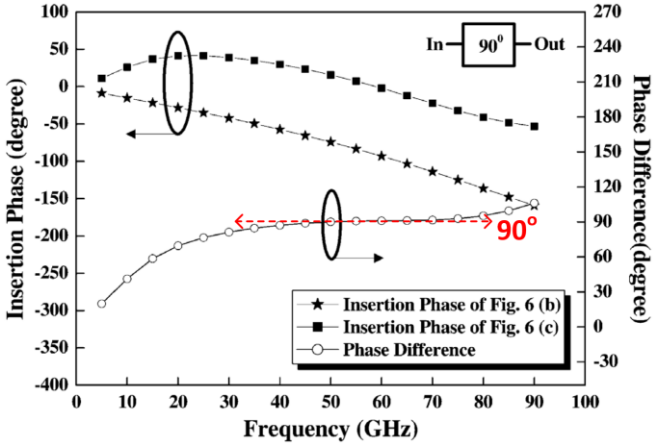


(a) (b)

Fig. 10. a) π-type switch-type phase shifter; b) T-type switch-type phase shifter [12].

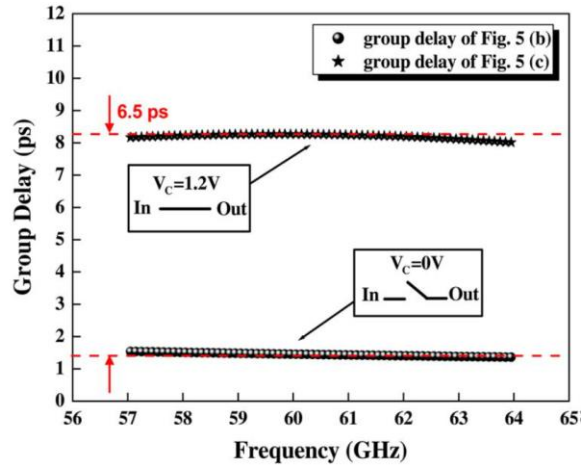


(a)

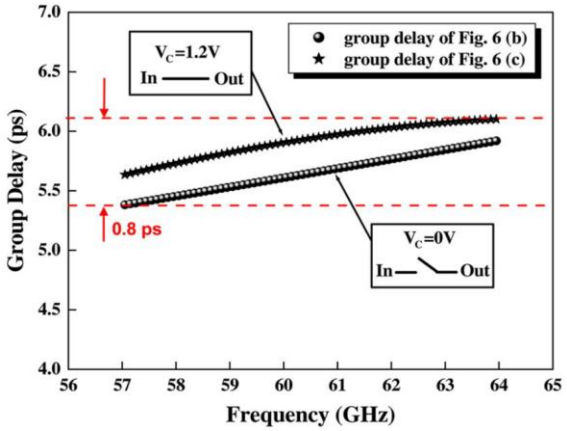


(b)

Fig 11. (a) shows phase difference of the π-type phase shifter; (b) shows the phase difference of the T-type phase shifter [12].



(a)



(b)

Fig 12. (a) shows the group delay of the π-type phase shifter; (b) shows the group delay of the T-type phase shifter [12].

In addition to using a 5-bit phase-variation phase shifter, we also implemented a low phase-variation three-stage VGA with a phase-compensation capacitor (C_x) and a source degeneration inductor (L_E) as shown in Fig. 8 to significantly reduce the phase variation from 10.5° to 1.5°.

This proposed 57-64-GHz low phase-error 5-bit switch-type phase shifter with an integrated low phase-variation VGA using 90-nm CMOS technology shows a combined root-mean-square (RMS) phase error of 3.3° at 63 GHz. The 5-bit phase shifter accounts for 2° of the measured RMS phase error at 62 GHz while the VGA can attain a gain tuning of 6.2 dB with a 1.86° phase variation, as shown in Fig. 13. Having a low phase-variation VGA that has small impact on the phase variation of the phase shifter makes this suitable for high-resolution phased arrays.

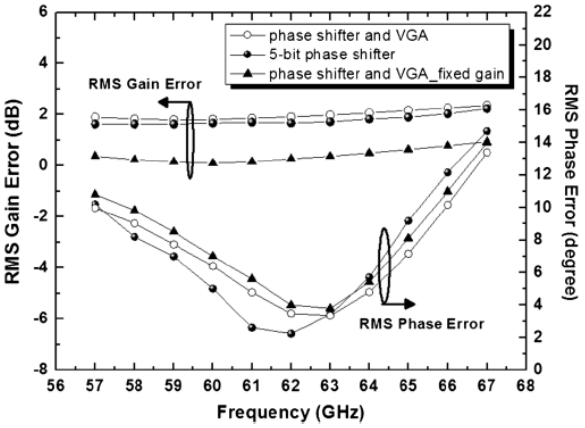


Fig. 13. RMS gain error and RMS phase error for 5-bit phase shifter and VGA [12].

V. QAM Calibration I: Millimeter Wave 1024-QAM Broadband I/Q Transmitter

When implementing a high QAM modulator, the most significant issues that impair the RF output are usually related to nonlinearity and I/Q mismatch. Achieving higher linearity can be improved by power back-off, but mitigating the I/Q mismatch can only be improved through topology selection and parasitic-insensitive design methodology. The calibration of I/Q mismatch can be divided into two parts: (1) PM calibration, and (2) AM calibration.

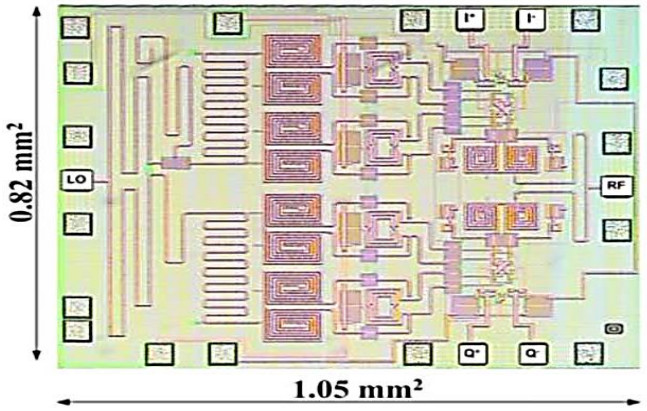


Fig. 14. Die photograph of the *E*-band modulator [14].

The I/Q calibration structure is implemented at the local oscillator (LO) port such that the I/Q balance is less sensitive to the loading effect from the RF port, as shown in Fig. 15. The proposed structure can compensate for both amplitude and phase distortion and can also achieve high Image Rejection Ratio (IRR) of the modulator over a wide bandwidth at high data rates. In the structure shown in Fig. 15, a LO broadband 45° power splitter when combined with amplitude and phase compensation for sub-harmonic I/Q modulator can then achieve a low-amplitude and phase-imbalanced structure.

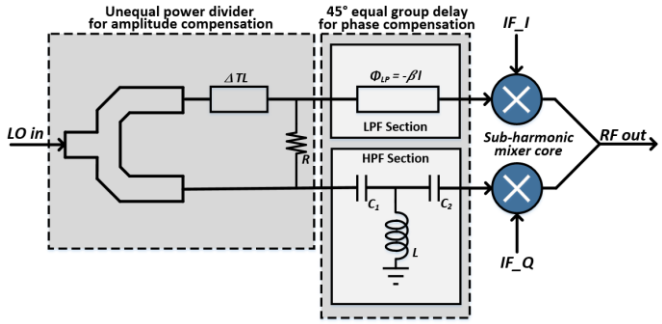


Fig. 15. A 45° phase shift power splitter with a delay line and HPF/LPF provides amplitude and phase compensation for I/Q calibration at the LO port [14].

For the I and Q mixer to have quadrature mixing, a LO signal power splitter with a 45° phase shift is used because the RF frequency is twice the LO frequency in the sub-harmonic mixer. A 45° phase shift with high-pass filter (HPF) and low-pass filter (LPF) structures is used to have low insertion loss, broad bandwidth, and low-imbalance 45° equal group delay. The power splitter also uses an amplitude compensation circuit to reduce the I/Q mismatch of the entire modulator.

For PM calibration, the combination of a HPF and a LPF was selected because the progressive phase of the HPF structure and the phase delay of the LPF structure can create the 45° phase difference between two output ports and create a broadband low-imbalance group delay, as shown in Fig. 15. When using the HPF and LPF design, amplitude imbalance will arise because the on-chip Metal-Insulator-Metal (MIM) capacitor, inductor, and transmission lines are not ideal. For AM calibration, a 50-µm delay line also shown in Fig. 15 is introduced to compensate for the amplitude imbalance. Due to the phase shift caused by the compensated transmission line length, the center frequency and the phase difference of the LPF and HPF design were slightly adjusted so that both phase and amplitude imbalance can be compensated at the same time.

For the proposed structure that contains both the HPF/LPF and the additional delay line, the amplitude imbalance is less than 0.04 dB and the phase difference is less than 0.5° from 32 to 45 GHz for the LO frequency, as shown in Fig. 14. The measured IRR is also more than 40 dBc for 64-84 GHz as shown in Fig. 16 and Fig. 17.

A digitally-controlled quadrature error correction circuit is proposed to lower the error vector magnitude (EVM) of a dual-band transmitter [15]. This error correction circuit consists of four VGAs with different gains as shown in Fig. 18. Each amplifier is controlled by 4 digital bits that adjusts the quadrature amplitude and phase mismatches. This correction stage is cascaded with the up-conversion mixer in the transmitter. With the error correction stage, the EVM of the transmitter is lowered from 3.21% to 2.8% for a 64-QAM at a 2.4-Ms/s symbol rate, and by more than 1% for 16-QAM at a 3-Ms/s symbol rate.

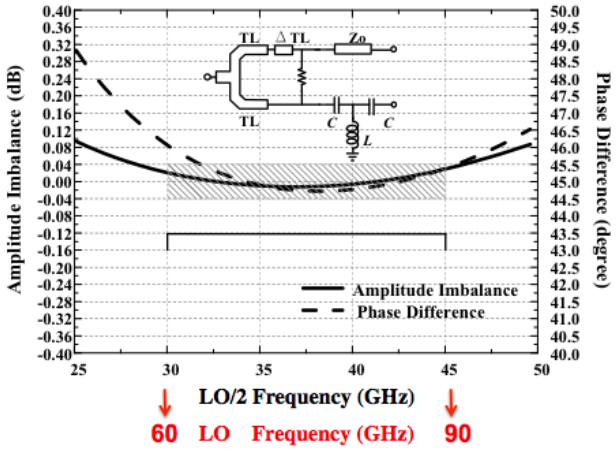


Fig. 16. Combining a delay line with HPF/LPF helps mitigate both the amplitude imbalance and phase difference [14].

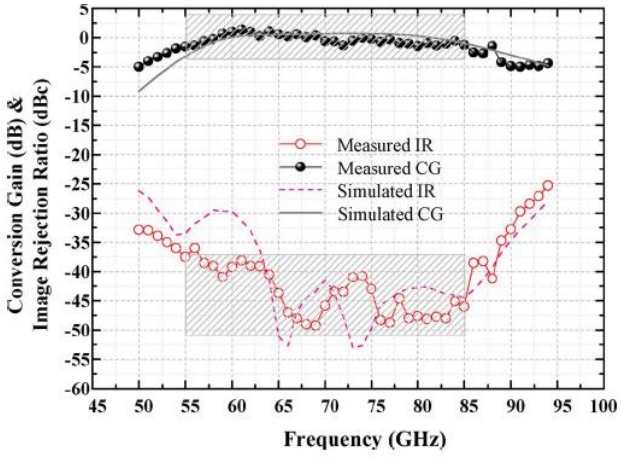


Fig. 17. Measured and Simulated Conversion Gain and Image Rejection of the *E*-band Modulator [14].

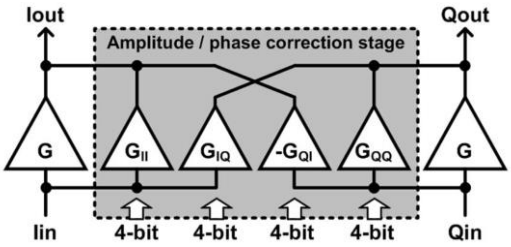


Fig. 18. Amplitude and phase correction using VGAs [15].

VI. QAM Calibration II: Self-Healing Broadband Transceiver

To further improve the performance of the smart RFIC, the mismatches and performance degradation due to environmental and process variations in a transceiver can be mitigated by some systematic and digitally-assisted approaches, such as built-in test (BIT) with automatic calibration circuits, or self-healing, that monitors the system performance in real time and employs knob control accordingly [16]-[25]. The accuracy of the sensors, the resolution of the tuning knobs, and the stability and settling of the feedback loop are critical to healing process. One example of a broadband receiver with BIT is shown in Fig. 19. During the self-healing process of the receiver that consists of a LNA and a mixer, on-chip frequency sources generate RF test signals to the device-under-test. With some feedback performance indicators from the on-chip sensors, the tuning knobs in both the LNA and the mixer circuit blocks can be adjusted to improve the noise figure (NF), linearity, gain, and image rejection.

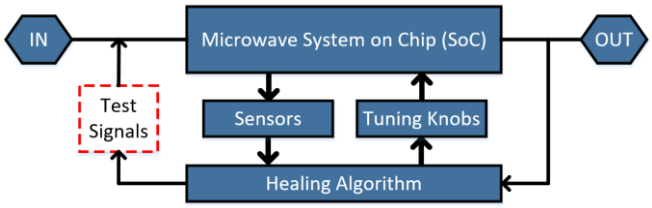


Fig. 19. Block diagram of a general BIT system showing the interconnection between signal sources, sensors, tuning knobs, and healing algorithm [16].

Specifically, in the receiver, tuning knobs control the dc biases of the LNA and mixer that are sensitive to PVT. The healing algorithm adjusts the tuning knobs to find the optimal value, as shown in Fig. 20. After the signals are down-converted, the biases of the VGAs can be tuned by making differential adjustments to it to change the gain of the quadrature paths, which improves the IRR from 26.7dB to 33dB, output third-order intercept point (OIP3) from 1.5dBm to 8.3dBm, NF from 12.2dB to 11.1dB, and gain from 26.9dB to 33.1dB, with healing.

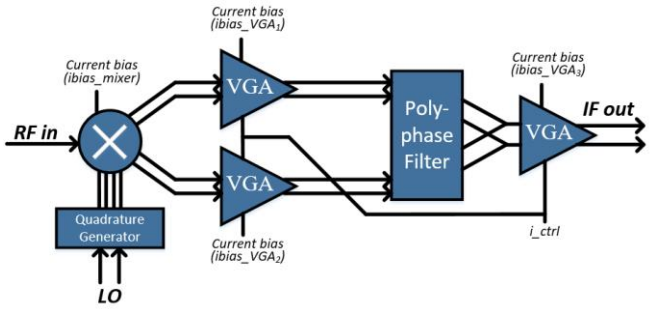


Fig. 20. 8-18-GHz tunable SiGe Image Reject Mixer [6].

In addition to tuning the dc bias knobs that optimizes NF, the impedance of the LNA is adjusted digitally to tune the frequency response of the amplifier. The whole self-healing LNA includes on-chip sensors, DACs, and digital controllers. With the self-healing technique, the standard deviation of NF is reduced by 37%, and the 3-dB bandwidth varies between 10.6 GHz and 12.5 GHz with different knob settings [21].

For healing the transmitter as shown in Fig. 21, the probe generator in the self-healing controller (SHC) creates test tones using the numerically controlled oscillators (NCOs). These test tones can have adjustable frequencies and amplitudes to probe the millimeter-wave transceiver and measure envelope variations, power level, and temperature from the transceiver impairments. From the performance metrics collected from a few different sets of test tones, coarse searching range and local minimum can be estimated. Fine search then can be performed around the local minimum to find the optimal spot. The parameter estimator (PE) which contains a 128-point fast Fourier transform (FFT) processor processes the sensor measurements. The controller then can dynamically change the rate of control for the tuning knobs from the reliability measures produced by the PE. The 1-dB compression point, third-order output intermodulation, and I/Q mismatch can be improved post healing.

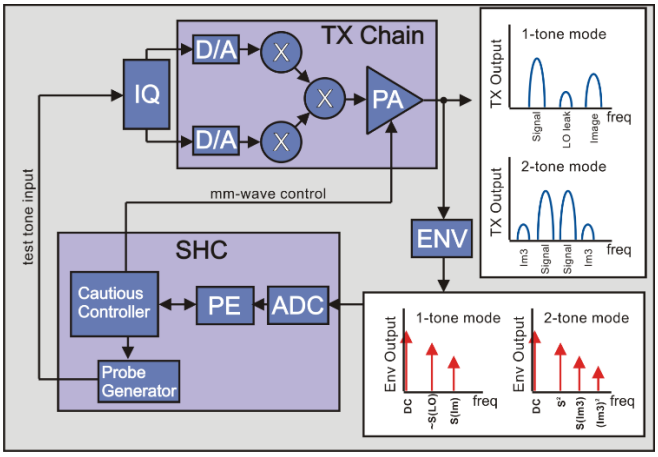


Fig. 21. Transmitter self-healing system showing adjustable transmitter chain, I/Q correction unit, envelope detector and SHC [17].

Fig. 22 shows the parameters of self-healing in the receiver. Initially, a low power reference test tone is generated and fed into the transmitter to characterize the gain and linearity of the transmitter as a calibration phase. Then, the transmitter's probe generator creates a two-tone. The de-imbedded Tx-to-Rx coupling then computes the

power delivered, which is detected using an envelope detector. Subsequently, the SHC′s FFT processor detects the tone amplitudes at the receiver output to find out the chain gain of the receiver, then finds the output noise when the transmitter is turned off. A temperature sensor then finds the thermal noise floor, so that the NF value can be computed to allow the bias current adjustments at each LNA stage.

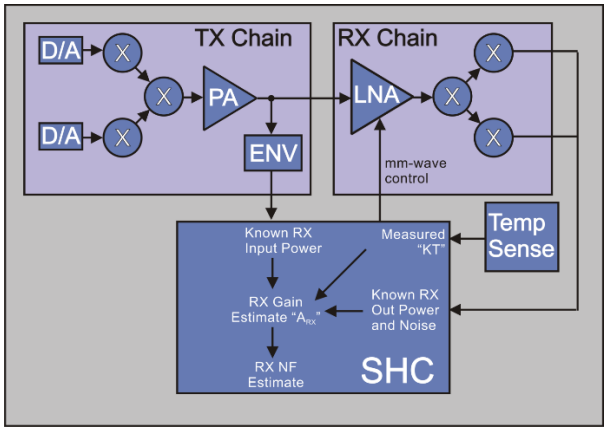


Fig. 22. Receiver self-healing system showing adjustable transmitter chain, adjustable receiver chain, temperature sensor, envelope detector and SHC [17].

By using an active self-healing broadband transceiver to calibrate QAM, the gain, NF, IRR, and OIP3 can all be improved post-healing. However, because the IRR only reaches 33 dB, only using this active QAM calibration with self-healing does not satisfy 1024 QAM, we will then combine this self-healing technique with the other mentioned calibration techniques to achieve 1024 QAM.

VII. Conclusion

A smart RFIC needs more user-defined functions and environmental sensors to respond to the changing world. A fast and low-powered frequency sensor is developed by using the Miller frequency divider. A digital DAC can improve the amplitude sensing accuracy. Broadband phase calibration can be implemented through HPF and LPF to achieve a broad bandwidth and low-imbalance equal group delay, within a phase error of 1° in a millimeter-wave frequency. Active QAM calibration through a self-healing technique can significantly improve the transceiver performance even under PVT variations.

References

[1] Y.-H. Kuo, J.-H. Tsai, T.-W. Huang, and H. Wang, "Design and analysis of digital-assisted bandwidth-enhanced miller divider in 0.18-μm CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 12, pp. 3769-3777, Dec. 2012.

[2] S. Moghadami, J. Isaac, and S. Ardalan, "A 0.2-0.3 THz CMOS amplifier with tunable neutralization technique," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 6, pp. 1088-1093, Nov. 2015.

[3] Y.-H. Kuo, J.-H. Tsai, and T.-W. Huang, "A digital-calibrated transmitter-to-receiver isolator in radar applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 12, pp. 651-653, Dec. 2012.

[4] C.-J. Jeong, Y. Sun, S.-K. Han, and S.-G. Lee, "A 2.2 mW, 40 dB automatic gain controllable low noise amplifier for FM receiver," *IEEE Trans. Circuits Syst–I: Regular Papers*, vol. 62, no. 2, pp. 600-606, Feb. 2015.

[5] J. Y.-C. Liu, Q. J. Gu, A. Tang, N.-Y. Wang, and M.-C. F. Chang, "A 60 GHz tunable output profile power amplifier in 65 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 377-379, Jul. 2011.

[6] U. R. Pfeiffer and D. Goren, "A 20 dBm fully-integrated 60 GHz SiGe power amplifier with automatic level control," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1455-1463, Jul. 2007.

[7] Y.-H. Lin and H. Wang, "A low phase and gain error passive phase shifter in 90 nm CMOS for 60 GHz phase array system application," in *IEEE MTT-S Int. Microw. Symposium Digest*, May 2016.

[8] F. Meng, K. Ma, K. S. Yeo, and S. Xu, "A 57-to-64-GHz 0.094-mm^2 5-bit passive phase shifter in 65-nm CMOS," *IEEE. Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 5, pp. 1917-1925, May 2016.

[9] C. W. Byeon and C. S. Park, "A low-loss compact 60-GHz phase shifter in 65-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 7, pp. 663-665, Jul. 2017.

[10] B. Sadhu, J. F. Bulzacchelli, A. Valdes-Garcia, "A 28GHz SiGe BiCMOS phase invariant VGA," in *IEEE Radio Frequency Integrated Circuits Symp.*, May 2016.

[11] D. Huang, L. Zhang, D. Li, L. Zhang, Y. Wang, and Z. Yu, "A 60-GHz 360° 5-bit phase shifter with constant IL compensation followed by a normal amplifier with ±1 dB gain variation and 0.6-dBm OP_{1dB}, " *IEEE Trans. Circuits Syst–II: Express Briefs*, vol. 64, no. 12, pp. 1437-1441, Dec. 2017.

[12] W.-T. Li, Y.-C. Chiang, J.-H. Tsai, H.-Y. Yang, J.-H. Cheng, and T.-W. Huang, "60-GHz 5-bit phase shifter with integrated VGA phase-error compensation," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 3, pp.1224-1235, Mar. 2013.

[13] Y.-C. Chiang, W.-T. Li, J.-H. Tsai, and T.-W. Huang, "A 60 GHz digitally controlled 4-bit phase shifter with 6-ps group delay deviation," in *IEEE MTT-S Int. Microw. Symposium Digest*, Jun. 2012.

[14] W.-H. Lin, H.-Y. Yang, J.-H. Tsai, T.-W. Huang, and H. Wang, "1024-QAM high image rejection E-band sub-harmonic IQ modulator and transmitter in 65-nm CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 11, pp. 3974-3985, Nov. 2013.

[15] P.-Y. Wu, A. K. Gupta, and J. F. Buckwalter, "A dual-band millimeter-wave direct-conversion transmitter with quadrature error correction," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 12, pp. 3118-3130, Dec. 2014.

[16] D. C. Howard, P. K. Saha, S. Shankar, T. D. England, A. S. Cardoso, R. M. Diestelhorst, S. Jung, and J. D. Cressler, "A SiGe 8–18-GHz receiver with built-in-testing capability for self-healing applications," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 10, pp. 2370-2380, Oct. 2014.

[17] A. Tang, F. Hsiao, D. Murphy, I-N. Ku, J. Liu, S. D'Souza, N.-Y. Wang, H. Wu, Y.-H. Wang, M. Tang, G. Virbila, M. Pham, D. Yang, Q. J. Gu, Y.-C. Wu, Y.-C. Kuan, C. Chien, and M.-C. F. Chang, "A low-overhead self-healing embedded system for ensuring high yield and long-term sustainability of 60GHz

4Gb/s radio-on-a-chip," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Digest*, Feb. 2012.

[18] S. M. Bowers, K. Sengupta, K. Dasgupta, B. D. Parker, and A. Hajimiri, "Integrated self-healing for mm-wave power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 61, no. 3, pp. 1301-1315, Mar. 2013.

[19] P. K. Saha, D. C. Howard, S. Shankar, R. Diestelhorst, T. England, and J. D. Cressler, "A 6-20 GHz adaptive SiGe image reject mixer for a self-healing receiver," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 1998-2006, Sept. 2012.

[20] E. J. Wyers, M. A. Morton, T. C. L. G. Sollner, C. T. Kelley, and P. D. Franzon, "A generally applicable calibration algorithm for digitally reconfigurable self-healing RFICs," *IEEE. Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 3, pp. 1151-1164, Mar. 2016.

[21] J.-O. Plouchart, F. Wang, A. Balteanu, B. Parker, M. A. T. Sanduleanu, M. Yeck, V. H.-C. Chen, W. Woods, B. Sadhu, A. Valdes-Garcia, X. Li, and D. Friedman, "A 18mW, 3.3dB NF, 60GHz LNA in 32nm SOI CMOS technology with autonomic NF calibration," in *IEEE Radio Frequency Integr. Circuits Symp.*, May 2015, pp. 319-322.

[22] A. Goyal, M. Swaminathan, A. Chatterjee, D. C. Howard, and J. D. Cressler, "A new self-healing methodology for RF amplifier circuits based on oscillation principles," *IEEE. Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 10, pp. 1835-1848, Oct. 2012.

[23] I.-T. Lee, Y.-T. Tsai, and S.-I. Liu, "A wide-range PLL using self-healing prescaler/VCO in 65-nm CMOS," *IEEE. Trans. Very Large Scale Integr. Syst.*, vol. 21, no. 2, pp. 250-258, Feb. 2013.

[24] M.-M. Mohsenpour and C. E. Saavedra, "Highly linear reconfigurable mixer designed for environment-aware receiver," *IEEE Int. Symp. Circuits Systems*, Sept. 2017.

[25] A. Rezola, J. F. Sevillano, I. Gurutzeaga, D. del Rio, R. Berenguer, I. Velez, "Built-in-self-calibration for I/Q imbalance in wideband millimeter-wave gigabit transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 11, pp. 4758-4769, Nov. 2017.