A 27-GHz Transformer Based Power Amplifier with 513.8-mW/mm^2 Output Power Density and 40.7% Peak PAE in 1-V 28-nm CMOS

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Abstract—**A fully integrated 27-GHz transformer based power amplifier with neutralization technique and low-loss transformer is proposed and fabricated in 28-nm CMOS technology. Several common-source cells are combined together as differential power cells. On-chip transformers and current-combining topology are used to combine amplifiers and reduce the problem of output power loss. Using an aluminium-pad (AP) layer on output matching reduces loss and can keep high PAE. In order to improve the overall stability, a neutralization structure is utilized in the combined cell. The measurement results demonstrate a small-signal gain of 13.1 dB, saturated power (P_{sat}) of 17.9 dBm, output power density of 513.8-mW/mm^2, and output 1-dB compression point (OP_{1dB}) of 14.7 dBm at 27 GHz. The peak power-added efficiency (PAE_{peak}) achieved by this power amplifier (PA) at 27 GHz is 40.7%. The core size of the chip is 0.12 mm^2. To the best of authors' knowledge, this circuit presents a superior power and efficiency performance compared with reported Ka-band common-source CMOS PAs.**

Keywords—**5G mobile communication, power amplifiers, transformers, CMOS integrated circuits.**

I. INTRODUCTION

To meet the growing demand for high-data-rate data transmission, the realization of fifth-generation (5G) wireless communication becomes a hot topic. 27 GHz is a candidate band for 5G application. Circuit and system designs for the lower millimeter wave (mm-wave) frequency band (27 GHz to 34 GHz) have been demonstrated recently [1]–[9]. Power amplifiers (PA) is one of the most critical building blocks among those designs. To achieve a high output power and power-added efficiency (PAE), an aluminium-pad (AP) layer is used during output matching. In order to reduce RF loss, current-combining topology has been used in previous work [10]. Capacitor-based neutralization has also been widely adopted in previous designs to improve overall stability [1]-[7]. In 5G wireless communication, a phased array transceiver is mainstream. Since the array system must consist of many antenna and transmitter modules as shown in Fig. 1, the size and performance of each component is important. Therefore, having a PA that is compact and also has high output power is very attractive for 5G applications.

In this paper, a 27-GHz integrated transformer-combined power amplifier with high power density is proposed. The concept using AP layer on output transformers decreases the insertion loss by 0.3 dB, enabling the current-combining PA to achieve higher output power and PAE. Hence, the optimized transistor sizes can be chosen to achieve a 17.9-dBm saturated

output power (P_{sat}), 513.8-mW/mm^2 output power density with a peak PAE of 40.7% at 27 GHz.
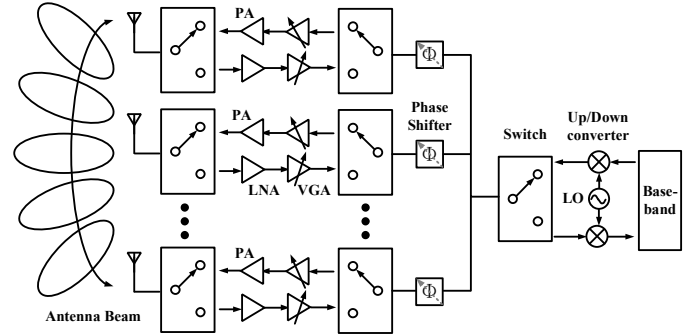

Fig. 1. Phased array transmitter for 5G communication system.

II. CIRCUIT DESIGN

The proposed circuit is fabricated in 28-nm CMOS process. This technology provides a single poly layer, nine metal layers (M1 to M9), and an AP layer for interconnection. Thick metal layers M8 and M9, are used to design transformers and transmission lines. The PA is composed of two differential amplifier cells with each cell consisting of a one-stage common source unit, as shown in Fig. 2.
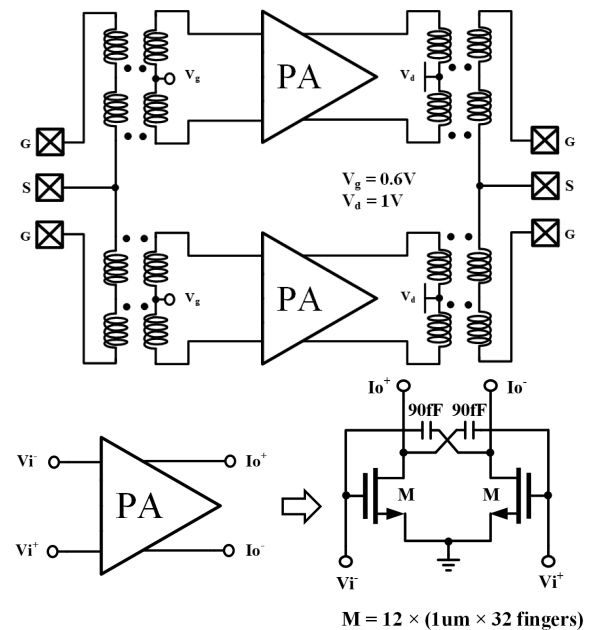

Fig. 2. Circuit schematic of the proposed PA

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \qquad (1)$$

By introducing skin effect (δ) from (1), the current flowing through the AP layer can be calculated, where ω is angular frequency, ρ is resistivity of the conductor, and μ is magnetic permeability.

Therefore, the output matching was fulfilled with the AP layer to reduce the loss and increase the PAE. Fig. 3 shows the output transformers with AP layer (orange layer).
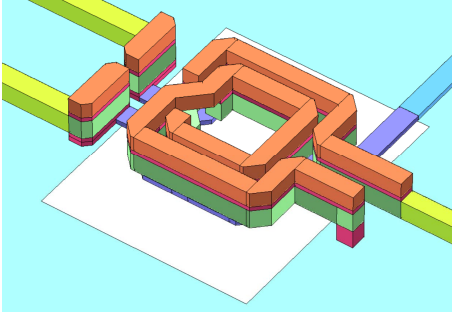

Fig. 3. 3D view of the output transformer with the AP layer.

Output transformers with an AP layer and output transformers without an AP layer were compared; the results show that with AP layer can decrease the insertion loss by 0.3 dB as shown in Fig 4. The lower insertion loss shows that the loss of the output transformer is reduced.
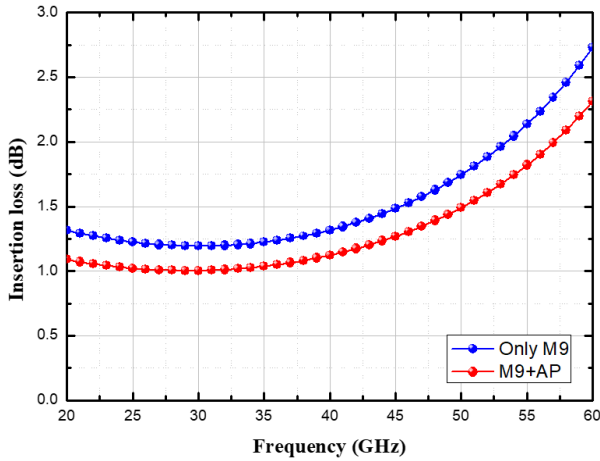

Fig. 4. Simulated result of the output transformer.

For the device selection, although choosing devices with large size can reduce the layout complexity, parasitic effects will degrade the efficiency and gain at mm-wave frequencies. Therefore, by carefully selecting proper transistor sizes and combining devices in parallel, high device intrinsic efficiency can be observed in the load pull simulation. Each transistor includes 32 fingers with a 1-μm width per finger. 12 transistors are then combined in each of the two power cells to increase the output power [2]. With this selection, the intrinsic device efficiency is about 68%. The device turning point of maximum stable gain (MSG)/maximum available gain (MAG)

curve is at 118 GHz at 1-V supply voltage. In order to improve the circuit stability, neutralization technique is applied. When the neutralization capacitance (C_{Neu}) is equal to gate-drain parasitic capacitance (C_{gd}), stability factor (K) can be maximized. The neutralization capacitor for a single CS device is 90 fF. The device turning point of MSG/MAG curve is changed to 15 GHz by including the C_{Neu}.

The optimal output load impedance (Z_{opt}) for each differential amplifier cell is 9.6 + j17.4 Ω at 27 GHz. The output transformers are designed to transform the Z_{opt} to 100 Ω and generate the differential signal. To increase the P_{sat}, the two differential amplifier cells are combined to transform the Z_{opt} to 50 Ω. All of the passive components are simulated using an EM simulator. Two differential amplifier cells are also designed to be as close as possible to reduce matching loss for layout considerations. For on wafer measurement consideration, the DC PADs were kept away from the RF PADs to avoid the probe collision.
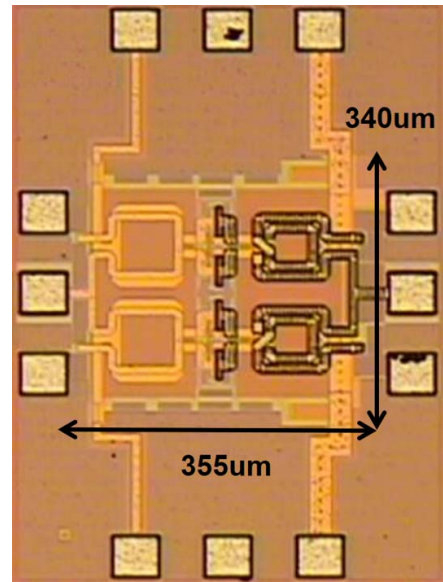
III. MEASUREMENT RESULT

Fig. 5. Chip micrograph with a core chip size of 355×340 μm².

The chip micrograph is shown in Fig. 5. The color of the output matching is darker than the input matching because of the added AP layer. The core size of the chip is 355×340 μm². This PA was measured using on-wafer probing with 1V supply voltage. Power dissipation is 56 mW under quiescent condition. The PA is checked through the spectrum analyzer and no oscillation power is observed. S-parameters are measured with an N5247A vector network analyzer with input power of -25 dBm. The simulation and measurement results agree with each other reasonably, as show in Fig. 6. The measured small-signal gain is 13.1 dB, and the output return loss is 11.2 dB for 27 GHz respectively. The large-signal power sweep is measured using an E8257D signal generator and an E4448A spectrum analyzer. Fig. 7 shows the simulated and measured output power, gain, and PAE at 27 GHz. The measured P_{sat}, output 1-dB compression point (OP_{1dB}), PAE_{peak} over different frequencies are shown in Fig. 8.

Table 1. Summary of the published Ka-band power amplifiers in CMOS process.

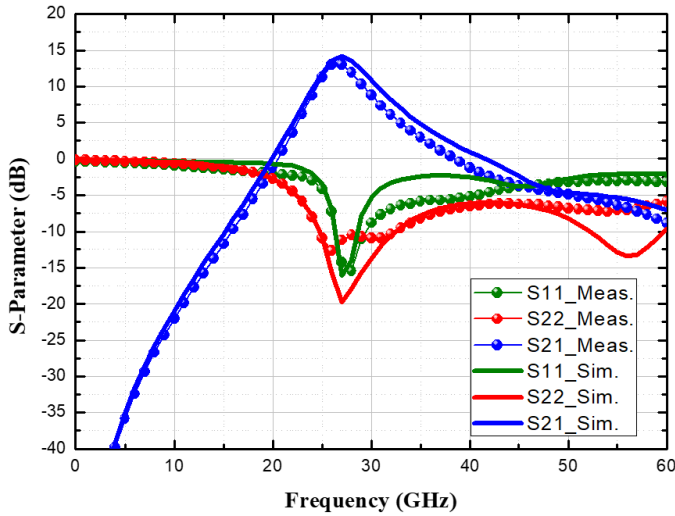| Reference	Process	Topology	Freq. (GHz)	Supply (V)	Gain (dB)	OP_{1dB} (dBm)	P_{sat} (dBm)	PAE_{peak} (%)	Area (mm²)	Power density (mW/mm²)
[9]	90nm CMOS	One-stage Cascode	28	2.4	16.3	23.2	26	34.1	0.401	992.8
[1]	28nm CMOS	One-Stage CS	28	1.1	10.0	14.0	14.8	36.5	0.28	107.9
[2]	28nm CMOS	Two-Stage CS	30	1	15.7	13.2	14	35.5	0.16	156.9
[3]	28nm CMOS	Two-Stage CS	34	1.1	20.8	13.4	16.6	24.2	0.16	285.7
[4]	40nm CMOS	Three-Stage CS	27	1.1	22.4	13.7	15.1	33.7	0.23	140.7
[5]	40nm CMOS	Two-Stage CS	27	1	20.5	16.8	18.1	41.5	0.36	179.3
[6]	65nm CMOS	Three-Stage CS	28	1	22.0	9.5	14.0	21.8	0.19	132.2
[7]	65nm CMOS	Two-Stage CS	32	1	20.8	12.9	15.3	32.9	0.11	308.1
[8]	65nm CMOS	Two-Stage CS	28	1.1	15.8	14	15.6	41	0.24	151.3
This work	**28nm CMOS**	**One-Stage CS**	**27**	**1**	**13.1**	**14.7**	**17.9**	**40.7**	**0.12**	**513.8**

Fig. 6. Measured *S*-parameters of the proposed PA.

Fig. 8. Measured power performance vs. frequency of the PA.
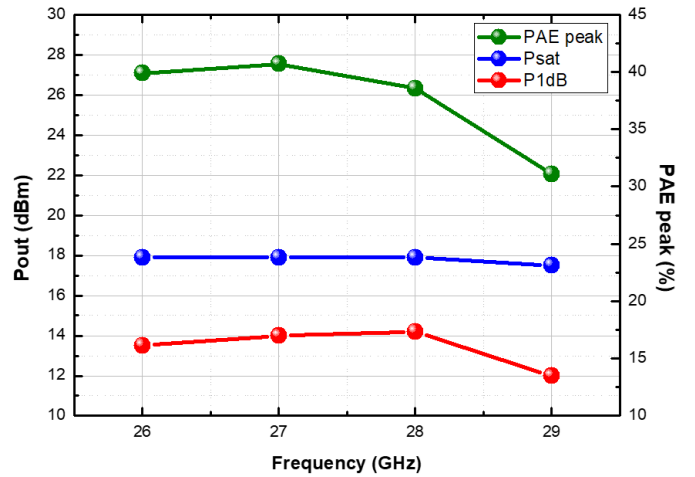

Fig. 7. Measured power performance of the proposed PA at 27GHz.

The measurement results demonstrate small-signal gain of 13.1 dB, P_{sat} of 17.9 dBm, OP_{1dB} of 14.7 dBm, and peak PAE of 40.7% respectively for 27 GHz shown in Fig. 7.

The third order inter-modulation distortion (IMD3) measured results at 27 GHz and 28 GHz are shown in Fig. 9. The frequency spacing of fundamental tone is 400 MHz. To keep the IMD3 below -30 dBc, the linear output power is 7.8 dBm at 27 GHz, while the linear output power is 7.1 dBm at 28 GHz. 10.1 dBm and 9.1 dBm linear output power can be obtained at 27 GHz and 28 GHz, respectively, when keeping the IMD3 below -25 dBc.

The application of the 5G communication requires a wide channel bandwidth, so a 400 MHz frequency spacing of fundamental tones was used. The results show that the low-side and high-side of the IMD3 are very close together, as shown in Fig. 9.
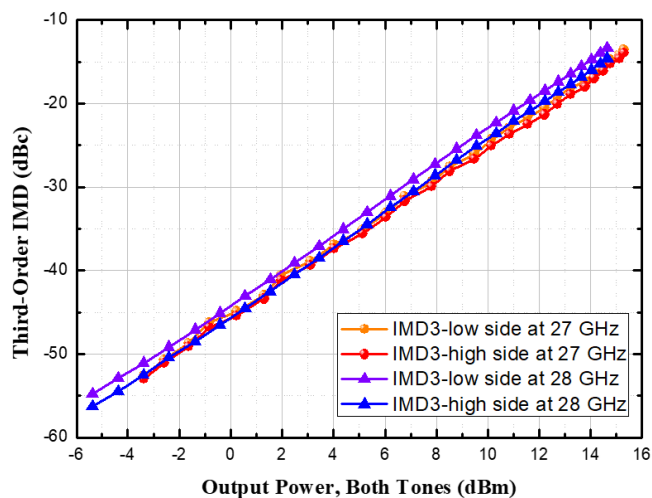
Fig. 9. Measured IMD3 of the PA at 27, 28 GHz.

IV. CONCLUSION

In this paper, a 27-GHz class-AB high efficiency power amplifier using 28-nm CMOS process is proposed. By using transformers and current-combining topology, the problem of imbalance can be mitigated. Neutralization is utilized on the combined power cells to improve stability. The measured results show 13.1-dB small signal gain, 17.9-dBm P_{sat}, and 40.7% PAE_{peak} at the frequency of 27 GHz. Table 1 is the summary of the published Ka-band power amplifiers in CMOS process. Although P_{sat} of this proposed PA is lower than P_{sat} of [5] and [9], power density is higher than [5] and PAE is higher than PAE of [9]. To the best of authors' knowledge, the proposed PA shows the highest power density performance (513.8 mW/mm^2) compared with the previous works under 1-V supply voltage, and the highest PAE (40.7 %) compared with the other PAs fabricated in the 28-nm CMOS process.

ACKNOWLEDGMENT

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