Reviews of High Image Rejection Up and Down Converters for Next-Generation Satellite Applications

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***Abstract*—In this paper, a review of high image rejection up- or down-converters is presented. Next-generation satellite applications need high uplink and downlink speeds, so a broadband design with a low image rejection ratio is important. By using a 0.18 μm CMOS single-quadrature architecture, this paper presents a 28-30GHz up-converter with a low-IF frequency range of 1.2 GHz and an IRR of <-38 dBc. Also presented is a 17-21 GHz down-converter with a low-IF frequency range of 2.2 GHz and a <-40 dBc IRR.**

Keywords—satellite, high image rejection, Ka-band, down-converter, up-converter

I. Introduction

Satellite communication has become more prevalent in people's lives as the demand increases. The need for a comprehensive coverage has also been growing as rural areas now also need a means of reliable communication. Having communication through satellite helps eliminate the difficulties of transmitting signal through rough terrain or weather, such as mountains or natural disasters. For the next generation Ka-Band satellite, it also can provide high data rates with a communication capacity above 1 Gbps. All these reasons lead to satellite communication becoming a more viable communication option, and so its demand has also risen. In recent years, many major players have entered this field such as WildBlue, Spaceway, ViaSat-1, and Hughes Jupiter with optimized payload for broad internet applications.

In order to achieve high speed satellite internet, there needs to be a broad bandwidth. The Ka-band satellite uplinks are currently set around 29 GHz and the downlink around 19 GHz, with roughly a 2 GHz bandwidth. Having low error vector magnitude (EVM) and low image rejection ratio (IRR) is crucial to achieving such high speeds; this can be achieved using common CMOS SoC architecture.

The traditional approach for image rejection is to place an image reject filter before the mixer. The use of the SAW filters imposes restrictions on the IC integration for the transceiver. Approaches which enable full monolithic integration of the radio include the Hartley and the Weaver architectures.

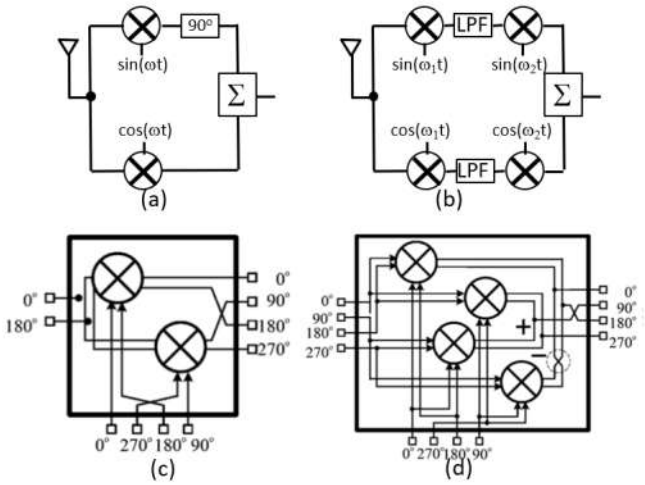

Fig. 1 (a) Hartley image rejection architecture, (b) Weaver architecture, (c) single-quadrature complex mixer, (d) double-quadrature mixer [1]

II. Image-Rejection for IC Integration

For IQ frequency converters, two identical mixers can mix the RF input with two quadrature phase LO to generate I-path, I(t), and Q-path, Q(t), as shown in Fig. 1. Since the image components in Q(t) are 90° out of phase with respect to those in I(t), If we shift I(t) or Q(t) by another 90° before adding them, the image may be removed, which is the Hartley image rejection architecture.

The main drawback of the Hartley architecture is its sensitivity to IQ mismatches, so Weaver architecture replaces the 90° phase shift network with quadrature mixing. The single/double quadrature architecture in Fig. 1 has the advantage of de-sensitizing the gain and phase imbalance of the I and Q paths, which can improve the image rejection capability.

III. Image-Rejection Up-Converters

This work presents a low-IF single-quadrature Hartley architecture that mixes two IF signals with a quadrature fundamental LO signal to output two RF signals, as shown in

Fig. 2(a). On the contrary, Fig. 2(b) shows an architecture that mixes the IF signals with a subharmonic LO quadrature generator into two sub-harmonic mixers to output RF signals.

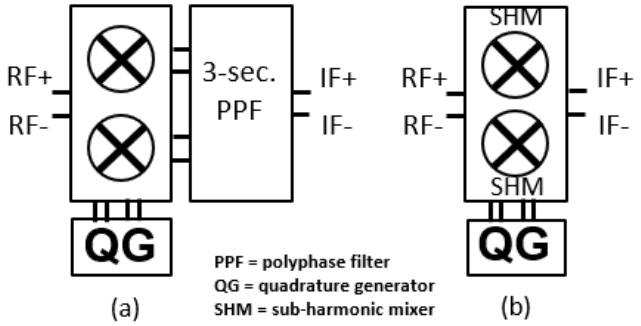

Fig. 2 (a) Single-quadrature modulator with polyphase filter, (b) Subharmonic single-quadrature modulator [2]

Fig. 3 shows two designs that have a quadrature LO input with an in-phase RF output combiner. Fig. 3(a) shows a balanced image-rejection mixer that mixes the LO signals with IF 0° and 90° signals. Fig. 3(b) shows the LO signal mixing with quadrature IF input over BPSK modulators to output two in-phase RF signals.

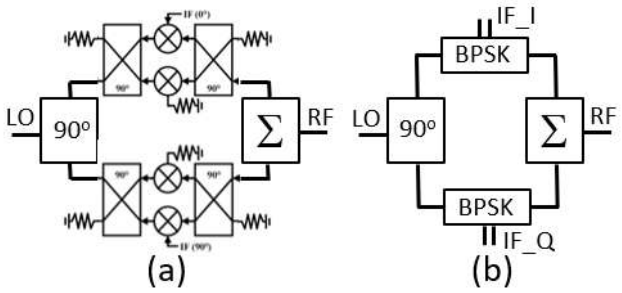

Fig. 3 (a) balanced image-rejection mixer [3] (b) IQ modulator using BPSK [4]

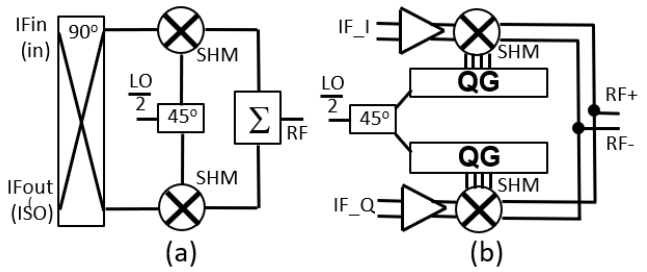

Fig. 4 (a) Sub-harmonic 45° modulator [5] (b) Sub-harmonic IQ modulator [6]

Fig. 4 shows a subharmonic 45° LO splitter that is mixed with a subharmonic mixer (SHM). Fig. 4(a) shows a single IF input that is mixed with the LO and outputs in-phase RF signals. Fig. 4(b) shows a quadrature IF input that is subharmonically mixed with a quadrature generated LO to output two RF signals.

Table I shows that the 29 GHz uplink can be realized by a 0.18 μm CMOS single-quadrature Hartley architecture. Its 1.2 GHz low-IF frequency range and its IRR of <-38 dBc across the 28-30 GHz bandwidth both increases its suitability for satellite communications application. [4] also has <-40 dBc IRR for 27-30 GHz with a low-IF frequency range of 5.9 GHz, which also is attractive for satellite applications.

TABLE I. COMPARISON OF UP-CONVERTERS

Ref.	Process	RF (GHz)	IF	IRR (dBc)
This Work #1	0.18 μm CMOS	28-30	0.95-2.15 GHz	< -38
[2]	0.13 μm CMOS	35-65	1 MHz – 3 GHz	< -30 @ 42-45 GHz
[3]	0.15 μm GaAs pHEMT	17-36	2 GHz (LO: 7.5-19 GHz)	N/A
[4]	0.13 μm CMOS	20-40	1 MHz – 6GHz	< -40 @ 27-30 GHz
[5]	0.3 μm GaAs MESFET	22.89-26.39	0.14GHz (LO: 11.4-13.1 GHz)	< -24
[6]	65 nm CMOS	64-84	5 MHz – 3 GHz	< -40

IV. Image-Rejection Down-Converters

The single-quadrature topology in Fig. 2(a) can be modified from an up-converter to a down-converter. In a similar fashion, the balanced image-rejection mixer in Fig. 3(a) can also be modified to a down-converter.

A unique down-conversion topology that can also be used is a Weaver image-rejection architecture as shown in Fig. 5. This single-quadrature weaver modulator monolithically integrates a three-stage LNA, down-converting mixers, and amplifier to improve the design's conversion gain and noise figure.

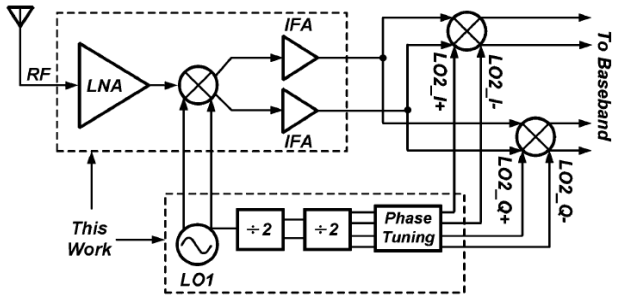

Fig. 5 Weaver image-rejection architecture [7]

Another down-conversion structure is shown in Fig. 6. The shown single-quadrature self-healing image-rejection down-converter mixes the RF input signal with a quadrature LO signal to output two IF signals after going through mixers,

VGAs, and a polyphase filter. By using these techniques, a broadband low IRR design can be realized.

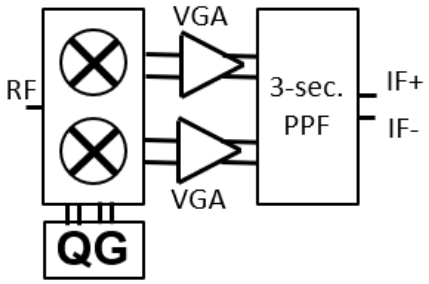

Fig. 6 Self-Healing image-rejection down-converter [8]

As can be seen from Table II, the 19 GHz Ka-band downlink can be realized by 0.18 μm CMOS single-quadrature Hartley architecture. The low-IF frequency range of 2.2 GHz and a <-40 dBc IRR are attractive for satellite applications.

TABLE II. COMPARISON OF DOWN-CONVERTERS

Ref.	Process	RF (GHz)	IF	IRR (dBc)
This Work #2	0.18 μm CMOS	17-21	1 MH – 2.3 GHz	< -40
[3]	0.15 μm GaAs pHEMT	15-35	2 GHz (LO: 6.5-18.5 GHz)	< -15
[7]	0.18 μm CMOS	23-25	3.82-5.82 GHz	< -44.8
[8]	0.2 μm SiGe BiCMOS	6-20	1.8 GHz	< -30

V. Conclusion

Single-quadrature converter can provide adequate bandwidth and low image rejection. The self-healing topology can enhance the single quadrature performance. IQ modulator using BPSK module provides a broad bandwidth with good IRR. A subharmonic 45º converter also has a flat broadband response. All these topologies are good candidates for satellite converter design.

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